This listing of claims replaces all prior versions, and listings of claims in the instant application:

Listing of Claims:

1. (Cancelled)

2-35. (Cancelled)

36. (Previously Presented) A method for arithmetic expression optimization, comprising:

receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base.

37. (Previously Presented) The method of claim 36, further comprising, after said converting said first instruction, returning to receiving said first instruction until all instructions defined for said first processor are converted.

38. (Previously Presented) The method of claim 36, further comprising rejecting an expression that cannot be optimized to a smaller base on said second processor.

39. (Previously Presented) The method of claim 36 wherein said first instruction is arithmetic.

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40. (Previously Presented) The method of claim 36 wherein said first instruction comprises a non-arithmetic, type-sensitive instruction.

41. (Previously Presented) The method of claim 36, further comprising linking each instruction to successor instructions in all control paths.

42. (Previously Presented) The method of claim 36 wherein said converting said first instruction further comprises:

linking each result of an instruction to all instructions that consume said result;

if said converting includes creating a value, linking said value to the instruction that produced said value; and

if said value carries a potential for overflow, linking said value to the instruction that originally caused said overflow.

43. (Previously Presented) The method of claim 36 wherein

said first processor comprises a Java™ Virtual Machine; and

said second processor comprises a Java Card™ Virtual Machine.

44. (Previously Presented) The method of claim 36 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

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said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size equal to the size of said at least one data type.

45. (Previously Presented) The method of claim 36 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size greater than the size of said at least one data type.

46. (Currently Amended) A method for arithmetic expression optimization, comprising:

receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

converting to a wider base a third instruction that is ~~the~~ a source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond a second base of a second processor and when said operator is sensitive to overflow, said third instruction having been previously optimized, said second base smaller than said first base, said wider base larger than said second base and smaller or equal to said first base.

47. (Previously Presented) The method of claim 46 wherein said converting to a wider base further comprises

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discarding previous conversion results of said third instruction before said converting to a wider base.

48. (Previously Presented) The method of claim 46, further comprising rejecting an expression that cannot be optimized to a smaller base on said second processor.

49. (Previously Presented) The method of claim 46 wherein said converting to a wider base further comprises rejecting said first instruction when said wider base is not supported by said second processor.

50. (Previously Presented) The method of claim 46 wherein said first instruction is arithmetic.

51. (Previously Presented) The method of claim 46 wherein said first instruction comprises a non-arithmetic, type-sensitive instruction.

52. (Previously Presented) The method of claim 46, further comprising linking each instruction to successor instructions in all control paths.

53. (Previously Presented) The method of claim 46 wherein

said first processor comprises a Java™ Virtual Machine; and

said second processor comprises a Java Card™ Virtual Machine.

54. (Previously Presented) The method of claim 46 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data

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type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size equal to the size of said at least one data type.

55. (Previously Presented) The method of claim 46 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size greater than the size of said at least one data type.

56. (Previously Presented) A program storage device readable by a machine, embodying a program of instructions executable by the machine to perform a method for arithmetic expression optimization, the method comprising:

receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base.

57. (Previously Presented) The program storage device of claim 56, said method further comprising, after said converting

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said first instruction, returning to receiving said first instruction until all instructions defined for said first processor are converted.

58. (Previously Presented) The program storage device of claim 56, said method further comprising rejecting an expression that cannot be optimized to a smaller base on said second processor.

59. (Previously Presented) The program storage device of claim 56 wherein said first instruction is arithmetic.

60. (Previously Presented) The program storage device of claim 56 wherein said first instruction comprises a non-arithmetic, type-sensitive instruction.

61. (Previously Presented) The program storage device of claim 56, said method further comprising linking each instruction to successor instructions in all control paths.

62. (Previously Presented) The program storage device of claim 56 wherein said converting said first instruction further comprises:

linking each result of an instruction to all instructions that consume said result;

if said converting includes creating a value, linking said value to the instruction that produced said value; and

if said value carries a potential for overflow, linking said value to the instruction that originally caused said overflow.

63. (Previously Presented) The program storage device of claim 56 wherein

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said first processor comprises a Java™ Virtual Machine; and

said second processor comprises a Java Card™ Virtual Machine.

64. (Previously Presented) The program storage device of claim 56 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size equal to the size of said at least one data type.

65. (Previously Presented) The program storage device of claim 56 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size greater than the size of said at least one data type.

66. (Currently Amended) A program storage device readable by a machine, embodying a program of instructions executable by the machine to perform a method for arithmetic expression optimization, the method comprising:

receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

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converting to a wider base a third instruction that is ~~thea~~ source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond a second base of a second processor and when said operator is sensitive to overflow, said third instruction having been previously optimized, said second base smaller than said first base, said wider base larger than said second base and smaller or equal to said first base.

67. (Previously Presented) The program storage device of claim 66 wherein said converting to a wider base further comprises discarding previous conversion results of said third instruction before said converting to a wider base.

68. (Previously Presented) The program storage device of claim 66, said method further comprising rejecting an expression that cannot be optimized to a smaller base on said second processor.

69. (Previously Presented) The program storage device of claim 66 wherein said converting to a wider base further comprises rejecting said first instruction when said wider base is not supported by said second processor.

70. (Previously Presented) The program storage device of claim 66 wherein said first instruction is arithmetic.

71. (Previously Presented) The program storage device of claim 66 wherein said first instruction comprises a non-arithmetic, type-sensitive instruction.

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72. (Previously Presented) The program storage device of claim 66, said method further comprising linking each instruction to successor instructions in all control paths.

73. (Previously Presented) The program storage device of claim 66 wherein

said first processor comprises a Java™ Virtual Machine; and

said second processor comprises a Java Card™ Virtual Machine.

74. (Previously Presented) The program storage device of claim 66 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size equal to the size of said at least one data type.

75. (Previously Presented) The program storage device of claim 66 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size greater than the size of said at least one data type.

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76. (Previously Presented) An apparatus for arithmetic expression optimization, comprising:

means for receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

means for converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base.

77. (Previously Presented) The apparatus of claim 76, further comprising means for, after said converting said first instruction, returning to receiving said first instruction until all instructions defined for said first processor are converted.

78. (Previously Presented) The apparatus of claim 76, further comprising means for rejecting an expression that cannot be optimized to a smaller base on said second processor.

79. (Previously Presented) The apparatus of claim 76 wherein said first instruction is arithmetic.

80. (Previously Presented) The apparatus of claim 76 wherein said first instruction comprises a non-arithmetic, type-sensitive instruction.

81. (Previously Presented) The apparatus of claim 76, further comprising means for linking each instruction to successor instructions in all control paths.

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82. (Previously Presented) The apparatus of claim 76 wherein said means for converting said first instruction further comprises:

means for linking each result of an instruction to all instructions that consume said result;

means for, if said converting includes creating a value, linking said value to the instruction that produced said value; and

means for, if said value carries a potential for overflow, linking said value to the instruction that originally caused said overflow.

83. (Previously Presented) The apparatus of claim 76 wherein

said first processor comprises a Java™ Virtual Machine; and

said second processor comprises a Java Card™ Virtual Machine.

84. (Previously Presented) The apparatus of claim 76 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size equal to the size of said at least one data type.

85. (Previously Presented) The apparatus of claim 76 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data

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type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size greater than the size of said at least one data type.

86. (Currently Amended) An apparatus for arithmetic expression optimization, comprising:

means for receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

means for converting to a wider base a third instruction that is ~~the~~a source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond a second base of a second processor and when said operator is sensitive to overflow, said third instruction having been previously optimized, said second base smaller than said first base, said wider base larger than said second base and smaller or equal to said first base.

87. (Previously Presented) The apparatus of claim 86 wherein said means for converting to a wider base further comprises means for discarding previous conversion results of said third instruction before said converting to a wider base.

88. (Previously Presented) The apparatus of claim 86, further comprising means for rejecting an expression that cannot be optimized to a smaller base on said second processor.

89. (Previously Presented) The apparatus of claim 86 wherein said means for converting to a wider base further

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comprises means for rejecting said first instruction when said wider base is not supported by said second processor.

90. (Previously Presented) The apparatus of claim 86 wherein said first instruction is arithmetic.

91. (New) The apparatus of claim 86 wherein said first instruction comprises a non-arithmetic, type-sensitive instruction.

92. (Previously Presented) The apparatus of claim 86, further comprising means for linking each instruction to successor instructions in all control paths.

93. (Previously Presented) The apparatus of claim 86 wherein

said first processor comprises a Java™ Virtual Machine; and

said second processor comprises a Java Card™ Virtual Machine.

94. (Previously Presented) The apparatus of claim 86 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size equal to the size of said at least one data type.

95. (Previously Presented) The apparatus of claim 86 wherein

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said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size greater than the size of said at least one data type.

96. (Previously Presented) An apparatus for arithmetic expression optimization, comprising:

at least one memory having program instructions; and

at least one processor configured to use the program instructions to:

receive a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

convert said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base.

97. (Previously Presented) The apparatus of claim 96 wherein said apparatus is further configured to, after said converting said first instruction, return to receiving said first instruction until all instructions defined for said first processor are converted.

98. (Previously Presented) The apparatus of claim 96, wherein said apparatus is further configured to reject an expression that cannot be optimized to a smaller base on said second processor.

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99. (Previously Presented) The apparatus of claim 96 wherein said first instruction is arithmetic.

100. (Previously Presented) The apparatus of claim 96 wherein said first instruction comprises a non-arithmetic, type-sensitive instruction.

101. (Previously Presented) The apparatus of claim 96 wherein said apparatus is further configured to link each instruction to successor instructions in all control paths.

102. (Previously Presented) The apparatus of claim 96 wherein said apparatus is further configured to convert said first instruction by:

linking each result of an instruction to all instructions that consume said result;

if said converting includes creating a value, linking said value to the instruction that produced said value; and

if said value carries a potential for overflow, linking said value to the instruction that originally caused said overflow.

103. (Previously Presented) The apparatus of claim 96 wherein

said first processor comprises a Java™ Virtual Machine; and

said second processor comprises a Java Card™ Virtual Machine.

104. (Previously Presented) The apparatus of claim 96 wherein

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said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size equal to the size of said at least one data type.

105. (Previously Presented) The apparatus of claim 96 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size greater than the size of said at least one data type.

106. (Currently Amended) An apparatus for arithmetic expression optimization, comprising:

at least one memory having program instructions; and

at least one processor configured to use the program instructions to:

receive a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

convert to a wider base a third instruction that is ~~thea~~ source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond a second base of a second processor and when said operator is sensitive to overflow, said third

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instruction having been previously optimized, said second base smaller than said first base, said wider base larger than said second base and smaller or equal to said first base.

107. (Previously Presented) The apparatus of claim 106 wherein said apparatus is further configured to convert to a wider base comprises discarding previous conversion results of said third instruction before said converting to a wider base.

108. (Previously Presented) The apparatus of claim 106 wherein said apparatus is further configured to reject an expression that cannot be optimized to a smaller base on said second processor.

109. (Previously Presented) The apparatus of claim 106 wherein said converting to a wider base further comprises rejecting said first instruction when said wider base is not supported by said second processor.

110. (Previously Presented) The apparatus of claim 106 wherein said first instruction is arithmetic.

111. (Previously Presented) The apparatus of claim 106 wherein said first instruction comprises a non-arithmetic, type-sensitive instruction.

112. (Previously Presented) The apparatus of claim 106 wherein said apparatus is further configured to link further comprising linking each instruction to successor instructions in all control paths.

113. (Previously Presented) The apparatus of claim 106 wherein

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said first processor comprises a Java™ Virtual Machine; and

said second processor comprises a Java Card™ Virtual Machine.

114. (Previously Presented) The apparatus of claim 106 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size equal to the size of said at least one data type.

115. (Previously Presented) The apparatus of claim 106 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data type, said at least one data type having a size less than the size of said first base; and

said second base is used by said second processor for performing arithmetic operations on said at least one data type, said second base having a size greater than the size of said at least one data type.

116. (Currently Amended) A smart card having a microcontroller embedded therein, the smart card comprising a virtual machine being executed by a microcontroller, the virtual machine executing a software application comprising of a plurality of previously optimized instructions, the instructions optimized by a method comprising:

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receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base;

the virtual machine comprising:

means for receiving optimized instructions, the optimized instructions being previously optimized for execution on a resource-constrained device; and

means for executing said instructions.

117. (Currently Amended) A smart card having a microcontroller embedded therein, the smart card comprising a virtual machine being executed by a microcontroller, the virtual machine executing a software application comprising of a plurality of previously optimized instructions, the instructions optimized by a method comprising:

receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

converting to a wider base a third instruction that is ~~the~~a source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond a second base of a second processor and when said operator is sensitive to overflow, said third instruction having been previously optimized, said second base smaller than said first base, said wider base larger than said second base and smaller or equal to said first base; ~~.~~

the virtual machine comprising:

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means for receiving optimized instructions, the optimized instructions being previously optimized for execution on a resource-constrained device; and

means for executing said instructions.

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